REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

1. Rejection of claims 1-3, 5, 7-10, 12, 14, 15:

Response:

Claim 1:

Claim 1 has been amended to overcome this rejection. Specifically, the limitation" each layout in the connection layer corresponding to each sub-circuit cell creates a connection between some of the sub-circuit blocks within each corresponding sub-circuit cell by selectively connecting the sub-circuit blocks within each corresponding sub-circuit cell, and short-circuits the rest of the sub-circuit blocks within each sub-circuit cell not connected together to DC bias voltages of the chip" has been added to claim 1. This limitation finds support in paragraph [0026] for instance, and no new matter is introduced. Acceptance of the amendment is politely requested.

The short-circuit between the sub-circuit blocks and the DC bias voltages is able to prevent the chip from being damaged by electrostatic discharge (ESD). Regarding US 5,858,817, Bansal only teaches creating the internal interconnections within the logic cells or within the input and output buffer cells, but he fails to teach or suggest short-circuiting the sub-circuit blocks to DC bias voltages of the chip. Therefore, claim 1 is patentably distinct from Bansal, and should be allowed. Reconsideration of claim 1 is politely requested.

Claims 2-3, 5, 7-8:

Claims 2-3, 5 and 7-8 are dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claims 2-3, 5 and 7-8 is politely requested.

Claim 9:

Claim 9 has been amended to overcome this rejection. Specifically, the limitation" each layout of the connection layer creates a connection between some of the sub-circuit blocks within each corresponding sub-circuit cell, and short-circuits the rest of the sub-circuit blocks within each sub-circuit cell not connected together to DC bias voltages of the chip" has been added to claim 9. This limitation finds support in paragraph [0026] for instance, and no new matter is introduced. Acceptance of the amendment is politely requested.

The short-circuit between the sub-circuit blocks and the DC bias voltages is able to prevent the chip from being damaged by electrostatic discharge (ESD). Regarding US 5,858,817, Bansal only teaches creating the internal interconnections within the logic cells or within the input and output buffer cells, but he fails to teach or suggest short-circuiting the sub-circuit blocks to DC bias voltages of the chip. Therefore, claim 9 is patentably distinct from Bansal, and should be allowed. Reconsideration of claim 9 is politely requested.

Claims 10, 12, 14-15::

Claims 10, 12 and 14-15 are dependent on claim 9, and should be allowed if claim 9 is found allowable. Reconsideration of claims 10, 12 and 14-15 is politely requested.

2. Rejection of claims 6 and 13 under 35 U.S.C. 103(a) as being unpatentable over Bansal and further in view of Maeda (US 6,052,014):

Response:

Claim6::

Claim 6 is dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claim 6 is politely requested.

Claim 13::

Claim 13 is dependent on claim 9, and should be allowed if claim 9 is found allowable. Reconsideration of claim 13 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Winston Hsu/ Date: 01.29.2008

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)